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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/998,756	12/03/2001	Jeff L. Hunter	TI-33109	6454

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EXAMINER	
RUTTEN, JAMES D	
ART UNIT	**PAPER NUMBER**
2192	

DATE MAILED: 05/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/998,756	HUNTER ET AL.	
	Examiner	Art Unit	
	J. Derek Rutten	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,13-18,21 and 22* is/are rejected.

7)☒ Claim(s) *3-12,19,20,23 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Acknowledgement is made of Applicant's amendment dated 7 March 2005, responding to the 5 October 2004 Office action provided in the rejection of claims 1-24, wherein claims 14-16 have been amended, and no claims have been canceled or added. Claims 1-24 remain pending in the application and have been fully considered by the examiner.

2. Applicant's arguments, see pages 16 and 17, filed 7 March 2005, with respect to the rejection(s)of claim(s) 1, 17, and 21 under 35 U.S.C. 102(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of "Computer Architecture: A Quantitative Approach" by Patterson et al. (hereinafter "Patterson") further in view of U.S. Patent 6,480,818 to Alverson et al. (hereinafter "Alverson"), further in view of U.S. Patent 6,011,920 to Edwards et al. (hereinafter "Edwards")..

Claim Rejections - 35 USC § 103

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 1, 17, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over prior art of record U.S. Patent 6,065,078 to Falik et al. (hereinafter "Falik) in view of "Computer Architecture: A Quantitative Approach" by Patterson et al. (hereinafter "Patterson") further in view of U.S. Patent 6,480,818 to Alverson et al. (hereinafter "Alverson"), further in view of U.S. Patent 6,011,920 to Edwards et al. (hereinafter "Edwards").

As per claim 1, Falik discloses:

A method for maintaining coherency of software breakpoints in shared memory when debugging a multiple processor system (Falik column 17 lines 28-67: "Synchronization is achieved by means of shared memory or shared semaphore."), *the method comprising the steps of:*

activating a first debug session associated with a first processor of a plurality of processors and at least a second debug session associated with a second processor of the plurality of processors (Falik column 2 lines 37-43: "FIG. 18 illustrates the overall architecture of a system 1800 including a multiprocessor integrated circuit (Normandy 1810) and a host computer (HOST 1820) having a debugger (1830a to 1830c) for each processor (1840a to 1840c) that interacts in a debugger interface module 1841, with a separate monitor executing on each separate processor.");

setting a first software breakpoint in a shared memory location in the first debug session (Falik column 5 lines 4-8: "Abort is used to stop a processor's execution flow in response to an event caused by the host 1820 (e.g., a user pressed an abort button) or another processor **reached a breakpoint** and a full system stop is desired to best observe the entire system status at the

time of the breakpoint." Note that in order to reach a breakpoint, it must have been previously set.) *and*

Falik does not expressly disclose *such that all debug sessions are notified of the setting or clearing of the breakpoint.*

However, in an analogous environment, Patterson teaches the "write update" protocol for ensuring cache consistency in a shared memory system. See the top of page 659: "The alternative to an invalidate protocol is to **update all the cached copies of a data item when that item is written.** This type of protocol is called a *write update* or *write broadcast* protocol." Also in an analogous environment, Alverson teaches that when setting a breakpoint in a system that consists of multiple debug sessions, or "nubs", all targets should be notified. See column 10 lines 14-20: "For example, a nub may need to be executed for each processor, or instead a single nub may coordinate all target threads across the multiple processors. In addition, if a separate copy of the target is created for each of the processors, then **when setting breakpoints the breakpoint will need to be added to each copy of the target.**" Further in an analogous environment, Edwards teaches the general concept of setting and clearing breakpoints. See column 2 lines 47-51: "This allows the instrumentation server to notify the debug engine of other events such as, attaching or detaching from an application, suspension of debug

operations against an application, **setting and clearing breakpoints.**"

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Falik's shared memory debugging with Patterson's teaching of cache coherency further with Alverson's teaching of breakpoint notifications and Edwards teaching of setting and clearing breakpoints. One of ordinary skill would have been motivated to provide notification regarding setting and clearing software breakpoint instructions in order to maintain cache coherency among a group of processors.

As per claim 17, Falik discloses:

A software development system (column 20 line 2 – column 22 line 7), *comprising:*

a memory storage system holding a software development tool program (Fig. 21);

a host computer connected to the memory storage system, the host computer operable to execute the software development tool program (Fig. 18);

a test port for connecting to a target hardware system, the hardware system being comprised of multiple processors with common shared memory and operable to execute an application program (Fig. 19 and Fig. 21).

All further limitations have been addressed in the above rejection of claim 1.

As per claim 21, Falik discloses:

A digital system (column 20 line 2 – column 22 line 7), *comprising:*

multiple processors with common shared memory for executing an application program (FIG. 21)*; and*

All further limitations have been addressed in the above rejection of claim 1.

5. Claims 2, 18, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik, Patterson, Alverson, and Edwards as applied to claims 1, 17, and 21 above, and further in view of "Code Composer – User's Guide" by Texas Instruments (hereinafter "Code Composer").

As per claim 2, the above rejection of claim 1 is incorporated. Falik does not expressly disclose a memory map. However, in an analogous environment, Code Composer teaches: *the step of creating a software memory map of the memory usage of a processor in the system to be debugged* (Code Composer page 7-1 paragraph 1). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Code Composer's method of using a memory map with Falik's multiple processors. One of ordinary skill would have been motivated to track which processors had control of which ranges of memory so that other processors would be restricted from modifying the contents of that range.

As per claim 18, the above rejection of claim 17 is incorporated. All further limitations have been addressed in the above rejection of claim 2.

As per claim 22, the above rejection of claim 21 is incorporated. All further limitations have been addressed in the above rejection of claim 2.

6. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Falik, Patterson, Alverson, and Edwards as applied to claim 1 above, and further in view of prior art of record "How Debuggers Work" by Rosenberg.

As per claim 13, the above rejection of claim 1 is incorporated. Falik does not expressly disclose a method of stepping over code. However, in an analogous environment, Rosenberg teaches the well known method of stepping over source code:

requesting that a software breakpoint in a shared memory location be stepped over or program execution resumed after hitting the breakpoint in a third debug session (This is inherent in debugging since the alternative is terminating the program. Further, see Figure 6.3.);

clearing the software breakpoint in the shared memory location in the third debug session such that all debug sessions are notified of the clearing of the breakpoint (bottom of page 41);

stepping a processor associated with the third debug session to the instruction after the shared memory location from which the software breakpoint was cleared (bottom of page 41); *and*

setting the first software breakpoint in the shared memory location in the third debug session such that all debug sessions are notified of the setting of the breakpoint (bottom of page 41).

Rosenberg further discusses synchronization and notification of processors by a debugger on page 203 under "Multiprocessor Breakpoint Issues".

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Rosenberg's teaching of single-stepping with Falik's debugger. One of ordinary skill would have been motivated to ease into a problem area of code in order to understand and evaluate the incrementally evolving state of the program. This can be accomplished with the single-step mechanism taught by Rosenberg.

7. Claims 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik, Patterson, Alverson, Edwards and Rosenberg as applied to claim 13 above, and further in view of prior art of record, Code Composer.

As per claim 14, the above rejection of claim 13 is incorporated. Falik discloses halting (column 5 lines 5-8). Falik does not expressly disclose searching a software memory map. However, Code Composer teaches searching a memory map for processors having read access to shared memory (Code Composer page 7.1 paragraph 1). Further, Rosenberg teaches halting after requesting and before clearing (page 41). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Rosenberg's teaching of halting and Tarui's teaching of a memory map with

Falik's debugger. One of ordinary skill would have been motivated to synchronize the execution of parallel processors during a halt condition in order to examine a snapshot of the state of a running process.

As per claims 15 and 16, the above rejection of claim 13 is incorporated. All further limitations have been addressed in the above rejection of claims 3 and 8, respectively.

Allowable Subject Matter

8. Claims 3-7, 8-12, 19, 20, 23, and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to J. Derek Rutten whose telephone number is (571) 272-3703. The examiner can normally be reached on T-F 6:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jdr

WEI Y. ZHEN
PRIMARY EXAMINER